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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,564	09/28/2004	Erik Petrus Antonius Maria Bakkers	NL02 0287 US	9573
24738	7590	08/29/2006		
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131				
			EXAMINER ANGADI, MAKI A	
			ART UNIT 1765	PAPER NUMBER

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/509,564

Applicant(s)

BAKKERS ET AL.

Examiner

Maki A. Angadi

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) 8 and 9 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6 is/are allowed.
- 6) ☒ Claim(s) 1-5 and 7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 9/28/2004.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction is required under 35 U.S.C. 121 and 372.

This application contains the following inventions or groups of inventions, which are not so linked as to form a single general inventive concept under PCT Rule 13.1.

In accordance with 37 CFR 1.499, applicant is required, in reply to this action, to elect a single invention to which the claims must be restricted.

Group I claim(s) 1-8 drawn to method of manufacturing nanowires

Group II claim(s) 9 drawn to an electronic device.

The inventions listed as Groups I and II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: Group II, claim 9 includes a limitation directed at a "device" which is not included in Group I claims 1-8. The device implicates other structures in addition to the claimed nanowire structures.

During a telephone conversation with Peter Zawilski on 8/11/2006 a provisional election was made **without traverse** to prosecute the invention of Group 1 claims 1-8. Affirmation of this election must be made by applicant in replying to this Office action. Claim 9 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claim 1-3 and 7-8 are rejected under 102(b) over Sheridan (EP 0544408).

As to claim 1, Sheridan discloses a method that reads on the process of manufacturing quantum wires/nanowires or quantum/nano dots (col.1, lines 1-7, col.8, lines 36-56), which includes the steps of providing a patterned etching mask (col.8, lines 57-58) at a surface of a semiconductor substrate (col.8, lines 10-12), and etching the semiconductor substrate (col.9, lines 1-3) so as to form nanowires in a direction substantially perpendicular to the surface of the semiconductor substrate (col.9, lines 4-10, Fig.5A), the semiconductor substrate includes a first layer (16) of a first material and a second layer (14) of a second material, the layers adjoin one another (Fig.3) (col.9 lines 10-14); and etching takes place through the first and the second layer for forming the nanowires such that the nanowires include a first region of the first material and a second region of the second material (col.9, lines 15-19, Fig.5 and Fig.5A).

As to claim 2, Sheridan discloses a method of p type doping for layer 14 and n-type doping for the layer 16 (Fig.5) (col.8, lines 13-23 and col.9, lines 8-10).

As to *claim 3*, Sheridan discloses the growth of second layer (16) is formed by epitaxial overgrowth or implantation, diffusion or other means (col.8, lines 23).

As to *claim 7*, Sheridan discloses a method that reads on the process of removing the nanowires after the etching of the substrate (col.10, lines 11-24).

Claim 8 is rejected in view of the rejection of claims 1-7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

Art Unit: 1765

U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 4 and 5 are rejected under 102(b) over Sheridan (EP 0544408) as applied to claim 1 above, in view of Giovine, *Nanotechnology, Vol.12, pages 132-135, (2001)*.

As to claim 4, Sheridan discloses first material as p-doped Si (14)(col.8, lines 10-11) and uses n-doped Si (col.8, lines 20-22) but is silent about the use of SiC or SiGe as the second material. However, Giovine discloses the use of Si/SiGe heterostructures in the formation of nanowires (col.1, page 132). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select Si/SiGe heterostructures in the formation of quantum wires or dots in the process used by Sheridan because Giovine illustrates that Si/SiGe heterostructures result in two dimensional systems that can be used in the fabrication of high-mobility quantum wires (col.1, page 132).

As to claim 5, Sheridan discloses a method that reads on the following steps: (i) a third layer (18) Fig.5A of a third material, (ii) the second layer lies sandwiched between the first layer and the third layer, (iii) etching through the first, second and the third layer to form the nanowire, such that the nanowires includes the first region (14), second region (16) and the third region (18) (col.8, lines 57-58 and col.9, lines 1-10, Fig 5A). Sheridan is silent about the thickness

of the third layer. However, Giovine discloses the thickness of third layer such as SiGe in the range of about 5-35 nm in thickness. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select thickness of the third layer in the process used by Sheridan because Giovine illustrates that Si/SiGe heterostructures in the thickness range 5-35 nm provide high current density and low field mobility (page 132).

Allowable Subject Matter

3. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of Sheridan does not disclose or suggest the use of third material as being identical to the first material.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jin (US Pub.No. 2004/0071951) discloses ultra-high density information storage media and methods for making the same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maki A. Angadi whose telephone number is 571-272-8213. The examiner can normally be reached on 8 AM to 4.30 PM.

Art Unit: 1765

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dr. Maki Angadi
Examiner, Art Unit 1765

NADINE NORTON
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ART UNIT 1765

